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1 Review?: Capacitive coupling (5 pts)

I was struck, recently, by how difficult an “old” topic like RC behavior can be, when it’s a little different from the standard case. Several students convinced me we need more practice on such early learning. Here’s a little workout on RC’s.

Below, a capacitor feeds a pulse into several alternative circuit elements. Please draw the voltage waveform at the point where the capacitor meets “X” for each case. Show time and voltage scales, and label significant points on your waveform. As usual, we’ll be happy with answers good to about 10%. Both $R_{IN_X}$ and $C_{IN_X}$ describe the effect of a $C$ and $R$ in parallel; the far end of each is tied to a fixed voltage; let’s assume that voltage is ground, just so all our drawings will look the same.

Please note that we’d like you to draw $V_{out}$, not $V_{cap}$.

![Figure 1: pulse, capacitively-coupled to various circuit fragments](image)

Here are the several alternatives for the circuit element labelled “X;”

1.1 Idealized next stage: $R_{IN_X} = \infty$, $C_{IN_X} = 0$

1.2 Mixed next stage: $R_{IN_X} = \infty$, but $C_{IN_X} = 0.001\mu F$
1.3 **Mixed next stage:** $R_{INX} = 100k, C_{INx} = 0$

1.4 **Mixed next stage:** $R_{INX} = 1k, C_{INx} = 0$

1.5 **Non-ideal next stage:** $R_{INX} = 100k, C_{INX} = 0.01\mu F$
2 Stability (3 points, total)

For each case, tell us which circuit is the more vulnerable of the two to parasitic oscillations, and why. Draw in the best protection against such parasitics.

2.1 amp; I-to-V (1 point)

![Figure 3: Transistor on right is used as photodiode](image1)

2.2 Long coaxial cable as load (1 point)

![Figure 4: Long coax cable as load](image2)

2.3 Two feedback circuits that include capacitors (1 point)

![Figure 5: Two circuits that include caps](image3)
3 Calculating $R_{out}$ for amplifier with stuff in the loop (2 points)

The gain curve shown in fig. 6 describes a ’411.

![Figure 6: ’411 gain curve](image)

Assume that the op amp of fig. 7 is a ’411.

![Figure 7: effect of feedback on $R_{OUT}$](image)

If beta for the power transistors used in the push-pull is 25, and the op amp’s (hardware-) $R_{OUT}$ (that is, apart from the effects of feedback) is 200Ω, what is the circuit’s $R_{OUT}$ at the following two frequencies:

3.1 100Hz

3.2 10kHz
4 What all that Op Amp Gain does for us (4.5 points, total)

4.1 Gain for non-ideal open-loop gain (but assume no phase shift) (2 points)

We use the Golden Rules to calculate gain if, say, we feed back one part in 100:

![Figure 8: Feed back 1%](image)

The Golden Rules rely on an assumption that op amp gain is very high (because, in Black’s words, “… improvements are attained in proportion to the sacrifice that is made in amplifier gain…”). Let’s see what happens as we assume several values for op amp open-loop gain, $A$, in the circuit drawn in fig.8.

We would like you to calculate the circuit gain for the circuit of fig.8, given several alternative values for $A$:

- for $A = 100$, what circuit gain?
- for $A = 1000$, what circuit gain?
- for $A = 100,000$, what circuit gain?

4.2 Gain for non-ideal open-loop gain (assume 90-degree lagging phase shift) (2.5 points, subtotal)

Op amp open-loop gain, $A$, not only falls with frequency, but also shows a 90-degree lagging phase shift, from a few tens of Hertz up.

At first glance this sounds like bad news. But it actually improves the results for circuit gain. It turns out that the results of §4.1 are gloomier than real life. Here, we’d like you to do some calculations to confirm this good news.

Design an amp… (0.5 point)

Design a non-inverting amp, gain = 20 (using the Golden Rules). Assume an ideal op amp, as usual.
Calculate gains, for finite $A$ (2 points)

...assuming no phase shift: What is circuit gain, if op amp $A = 100$, with no phase shift (as assumed in §4.1)?

...assuming -90-degree phase shift:

What is circuit gain, if we acknowledge the phase lag, and describe the open-loop gain as $A = -100j$?\(^1\)

5 PID Questions (3 pts)

Motor-to-pot Loop Problem? (1 pt) What, most fundamentally, makes our motor-to-pot drive loop different from the other feedback loops we have set up with op amps, in many earlier labs? (There must be some difference—because ordinarily our loops are stable without this extra circuitry!)

5.1 Why “D”? (1 pt)

Briefly, why does adding a derivative of the error to the quantity that is fed around the loop help to stabilize the loop, when the amount of derivative is chosen judiciously?

\(^1\)This is weirdly mathy for this mathless course. But we thought the result might please you. The process is to clean up the messy expression for gain by 1) getting the ugly “$j$” out of the denominator by multiplying by the “complex conjugate” (see AoE, p. 34, for an example); then, 2) find the magnitude of the resulting complex number ($= \sqrt{\text{real}^2 + \text{imaginary}^2}$).
5.2 How much derivative? (1 pt)

Suppose that you saw your motor-control loop showing a “natural oscillation” frequency of 4Hz. What \( RC \) would you give the differentiator (assuming the “Proportional” gain was one—so that all circuit gain was applied, as in our lab circuit only after summing the \( P \) and \( D \) signals)? (Try to explain informally rather than by citing a magical rule of thumb.)

6 Automatic Gain Control (6 points, total)

An AGC holds its output amplitude roughly constant, as input amplitude varies. An AGC is essential in a car radio, because signal strength varies widely (there it is used on the radio-frequency signal); it is useful for simple voice tape recorders. Here, we’ll ask you to design such a circuit².

**Voltage-controlled resistance**

In order to make an amplifier whose gain can be controlled automatically, it is useful to have as a building block, a voltage-controlled resistance (let’s call this a “VR,” for short). This is a circuit one can build with a JFET and an op amp. Since the course did not treat JFETS, this term, we are not asking you to design anything using one; instead, we present you with a circuit that does the job, and we tell you its approximate transfer characteristic. Here it is:

![Figure 9: JFET as voltage-controlled resistance](image)

Note that this circuit works pretty well only for \( V_{DS} \leq \approx 0.1V \).

6.1 Variable-gain Amplifier (2 points)

Given such a VR, design an op amp non-inverting amplifier whose gain can be varied over at least the range 10 to 100 (to 10%), as \( V_{\text{CONTROL}} \) varies.

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²Paul H thought this question was too hard for the undergrads; but I think you can do it.
6.2 Peak Detector (2 points)

Now design a circuit that detects the peak or maximum level of a signal, and holds it, allowing the level to decay away (to about 1/e, or 37%) in 1 s. Let the circuit hide or compensate for any diode drop that would mar a simpler peak detector.3

6.3 Put the pieces together: AGC (2 points)

Now put your circuit fragments together—plus other circuitry you think is required—to make an AGC: a circuit that holds its output amplitude at about 1 volt, as input amplitude varies over a range 1V to 10V; \( R_{\text{OUT}} \) for the signal source is \( \leq 1\kappa\Omega \). You need not redraw the Variable-gain Amplifier; you may show it as a black box. This black box has an Signal Input, Signal Output, and gain Control input. Make sure that the input voltage to your VR does not exceed its range.

A fine point: It turns out to be wise to use not a bare op amp but a differential amp of modest gain (say, 10),4 to compare the reference voltage of 1V with the average amplitude. This is a fine point, perhaps, but maybe worth noticing, since you know about control loops that require similarly-modest gains (and no odd phase shifts) to maintain stability: the recent PID loop of Lab 10.

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3In the completed AGC loop, just below, this feature may not be necessary: or is it?. What do you think? At this point you probably haven’t an opinion, but you might reconsider the question when you’ve done §6.3, (“Put the pieces together: AGC”).

4You can even get by with no amp at all, relying on the gain of the JFET VR. But please draw us an amp anyway; it makes the circuit schematic more intelligible.