CANBERRA

DELAY AMPLIFIER
Model 1457

Operator's Manual

Physics 191/247 laboratory

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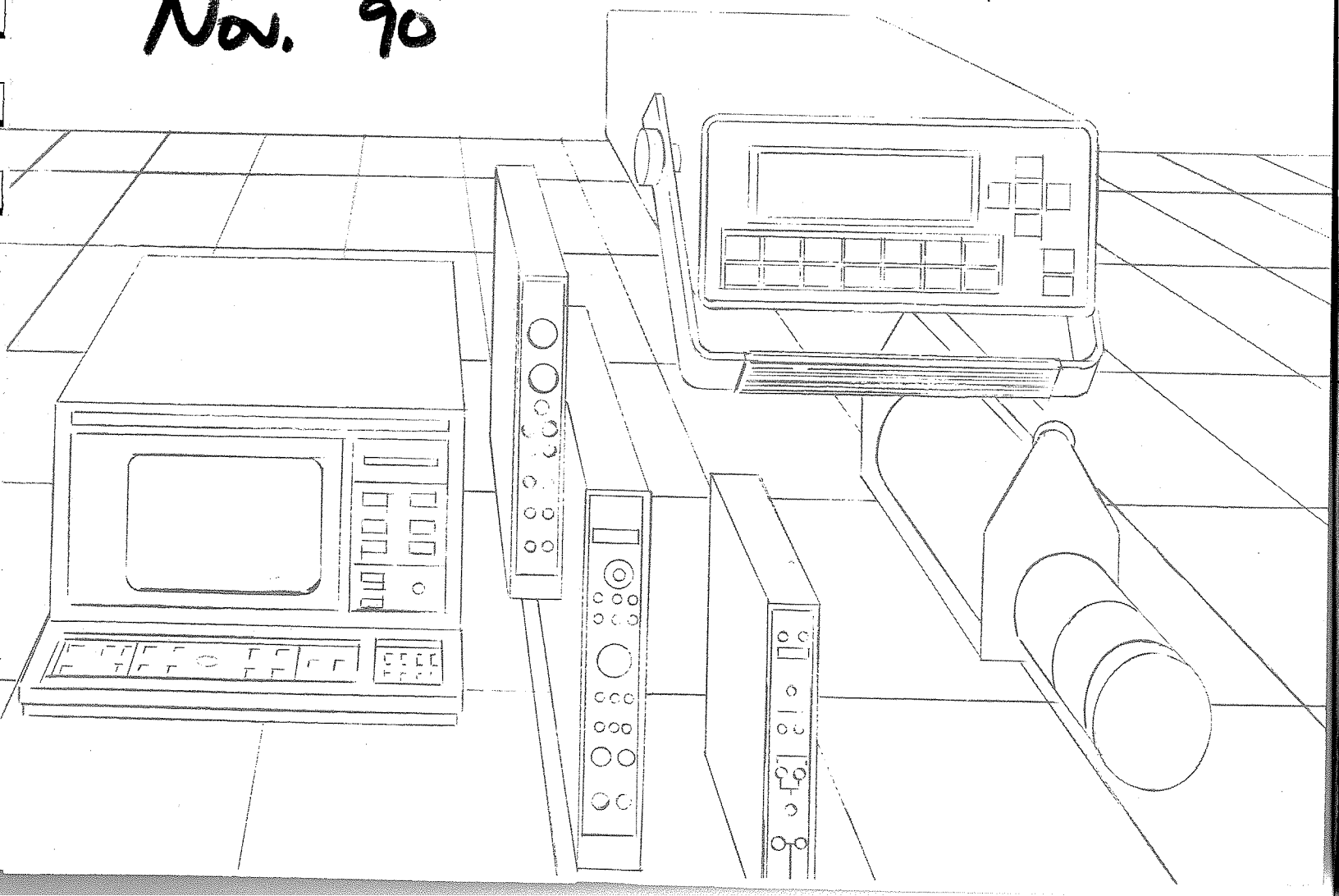

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Section 1
INTRODUCTION

The Canberra Model 1457 Delay Amplifier can delay logic or linear signals, from zero to 4.75 microseconds in 0.25 microsecond steps. The Delay Amplifier has a nominal gain of unity, adjustable by front panel control. The input signal may be of either polarity and an inverted or non-inverted output may be selected by means of a front panel switch.

The output full scale signal range is selected by a front panel control to be 3, 5, or 10 volts for a ten volt input signal.

The amount of delay is switch-selected by inserting any combination of five delay lines (0.25, 0.5, 1.0, 1.0, or 2.0 microseconds) in series with the signal of interest. The Model 1457 is DC coupled to give optimum performance at high count rates. The output DC level is adjustable by front panel control.

Section 2

SPECIFICATIONS

2.1 INPUT

INPUT	Amplitude: positive or negative 0 to 10 volt signal Impedance: greater than 1000 ohms, DC coupled
OUTPUT	Amplitude: positive or negative; delay and amplitude determined by front panel switch settings Delay: any combination of 0.25, 0.5, 1.0, 1.0, or 2.0 microseconds Impedance: less than 1 ohm, DC coupled

2.2 PERFORMANCE

LINEAR DELAY	Any combination of 0.25 0.5, 1.0, 1.0, and 2.0 microseconds
GAIN VARIATION WITH DELAY	±4% maximum for any combination of delays (2.0 microsecond Gaussian shaped pulse)
FEEDTHROUGH AND DELAY RIPPLE	Less than 1% (1.0 microsecond Gaussian shaped pulse)
MINIMUM ZERO DELAY	150 nanoseconds
DELAY TOLERANCE	±5%

RISE TIME AS A FUNCTION OF DELAY

DELAY (microseconds)	RISETIME (nanoseconds)
0	200
0.5	400
1.0	420
2.0	450
4.0	500

TEMPERATURE STABILITY	Gain shift: less than 0.003%/^{o}C/μsec delay
LINEARITY	Integral non-linearity: less than ±0.05% from 0.1 to 10.0 volts
DC LEVEL STABILITY	Better than 0.5mV/^{o}C at nominal 0VDC

2.3 CONNECTORS

INPUT	Front panel BNC UG-1094/U
OUTPUT	Front panel BNC UG-1094/U

2.4 POWER

+24VDC –	35mA	+12VDC –	15mA
-24VDC –	45mA	-12VDC –	15mA

2.5 PHYSICAL

SIZE	Standard single width module (1.35 inches wide) per TID-20893
WEIGHT	2.2 lb.

Section 3

CONTROLS AND CONNECTORS

DELAY
Five pushbuttons capable of selecting 5 individual delay times (0.25, 0.5, 1.0, 1.0 and 2.0 microseconds). They may be used individually or in combination with each other for other delay times.

RANGE
A three-position switch which provides a 0 to 10 volt, 0 to 5 volt, and 0 to 3 volt output for a 10 volt input. This provides the unit with three gain positions: 1, 1/2, and 1/3.3.

DC OFFSET
A screwdriver adjustment, single-turn potenticmeter for providing a DC offset voltage at the OUTPUT. The voltage is variable from -2 volts to +2 volts.

INPUT
Accepts positive or negative linear signal from 0 to 10 volts in amplitude. The input impedance is greater than 1000 ohms, DC coupled.

POLARITY
A two-position switch which selects the polarity of the OUTPUT signal.

GAIN
A screwdriver adjustable, single-turn potentiometer for compensating for any gain losses created by the delay line when it is switched into the circuit.

OUTPUT
Provides positive or negative signals with amplitudes of up to 10 volts (determined by front panel switch) and delayed by up to 4.75 microseconds (determined by front panel pushbuttons); output impedance less than 1 ohm, DC coupled.

Section 4

OPERATING INSTRUCTIONS

4.1 GENERAL

The purpose of this section is to familiarize the user with the controls of the Model 1457 Delay Amplifier and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

4.2 INITIAL OPERATION

4.2.1 Setup

1. Insert the Model 1457 Delay Amplifier in an AEC compatible base unit/power supply such as Canberra Model 2000. Set the Power switch to ON.

2. Connect the output from a pulse shaping amplifier (such as a Canberra Model 2010) to the INPUT connector of the Model 1457 using a "tee" connector. Simultaneously observe the amplifier (Model 2010) output on an oscilloscope (5V/cm. 1μsec/cm) or observe the amplitude on a multichannel analyzer.

3. Set RANGE switch on the Model 1457 to 10V.

4. Set POLARITY switch to POS.

5. Check that all DELAY pushbuttons are in the OUT position.

6. Connect the output of the Model 1457 to a second input on the oscilloscope (5V/cm, 1μsec/cm).

4.2.2 Initial Checkout

1. Slowly increase the amplifier signal (Model 2010) until a 10 volt peak signal is observed on the output of the Model 2010. Observe the output of the Model 1457 Delay Amplifier. It should be identical to the signal at the INPUT (output of the Model 2010) except for a possible difference in amplitude and offset voltage.

2. With a screwdriver, adjust the GAIN control on the front panel from one extreme to the other. Notice that the output amplitude varies above and below the input amplitude (10 volts). Now adjust the GAIN control so that the output amplitude is 10 volts.

3. Remove the input signal and observe the output with the oscilloscope (in a DC input mode) or a voltmeter. With a screwdriver, slowly adjust the DC OFFSET control on the front panel from one extreme to the other. Notice that the DC voltage on the output goes from approximately -2 volts to +2 volts. Adjust the DC offset capacitor for zero volts DC on the output.

4. Connect the Model 2010 back to the INPUT of the Model 1457 (still a 10 volt peak signal being applied). Change the position of the RANGE switch from 10V to 5V and notice that the output has changed from 10 volts to 5 volts. Change the range to 3V. The output signal is now 3 volts. Return the RANGE switch to the 10 volt position.

5. Change the position of the POLARITY switch from POS. to NEG. Observe that the output polarity also changes. Return the switch to the POS. position.

6. Observing both input and output signals, depress the 2μSEC DELAY pushbutton on the front panel. Observe that the OUTPUT signal is now delayed from the INPUT signal by 2μsec. Repeat for other values of DELAY. Notice that if two or more switches are depressed at the same time, the total delay time is the sum of the corresponding values of the switches depressed.

Section 5

THEORY OF OPERATION

5.1 GENERAL

Refer to Schematic Diagram D-12306 for use with the following discussions. Also see Figure 1 for the block diagram of the Model 1457.

The Model 1457 consists of an input amplifier, a delay line section, and an output amplifier. Refer to the block diagram.

5.2 INPUT AMPLIFIER

The input amplifier is used to match the impedance of the delay line and to compensate for any losses caused when the delay line is switched into the circuit. The gain compensation is accomplished by varying the closed loop gain of the amplifier (Q1-Q7) with the GAIN adjustment (RV-1). RV-1 is a portion of the amplifier's input resistance, therefore, when it is changed, the gain of the amplifier is changed:

$$\frac{\text{R feedback}}{\text{R input}} = \text{Gain}$$

The output impedance of the amplifier is 250 ohms looking into the delay line. The delay line itself has an impedance of 250 ohms also. Therefore, the output impedance of the amplifier is matched to the impedance of the delay line which gives minimum pulse reflections.

The input of the amplifier is a differential pair (Q6) and a current source (Q7). This provides a high input impedance. The output of Q6 is fed to two more current sources, Q2 and Q5. These provide high impedance, high gain and fast switching. The output from this amplifier goes to an FET (Q4) which in turn drives a complementary pair (Q1, Q3). These provide a low impedance output and fast switching.

5.3 DELAY LINE SECTION

The delay line consists of five separate delay lines which can be switched in and out of the circuit to provide the desired amount of delay. The five separate delays are 0.25, 0.5, 1.0, 1.0, and 2 microseconds. Any combination of these delay lines may be inserted in series by depressing the front panel pushbutton switches.

The output of the delay lines are also terminated by the impedance of the line to minimize reflected pulses caused by an impedance mismatch. This terminating resistance is made up of a voltage divider which yields three different ranges. These ranges give the total amplifier a gain of 1, 1/2, and 1/3.3 by means of a front panel RANGE switch. This RANGE switch selects either the 10V, 5V, or 3V range by selecting different points on the voltage divider and feeding it to the output amplifier.

5.4 OUTPUT AMPLIFIER

The output amplifier provides a low impedance output and a means of applying a DC offset voltage to the output. This amplifier has a fixed closed loop gain of approximately two, which compensates for the voltage division caused by impedance matching of the delay line at the input and output.

The DC offset is developed across a voltage divider, with a portion of this voltage being picked off RV-2 and presented to the amplifier. This DC voltage passes through the amplifier and is presented to the output BNC. It can be adjusted from -2 volts to +2 volts by means of the DC OFFSET adjustment (RV-2).

The POLARITY switch selects a positive or negative output polarity by feeding the output from the delay line to the inverting or non-inverting input of the output amplifier. The output impedance of the amplifier is low since the output stage of the amplifier is a complementary pair (Q8, Q12)..

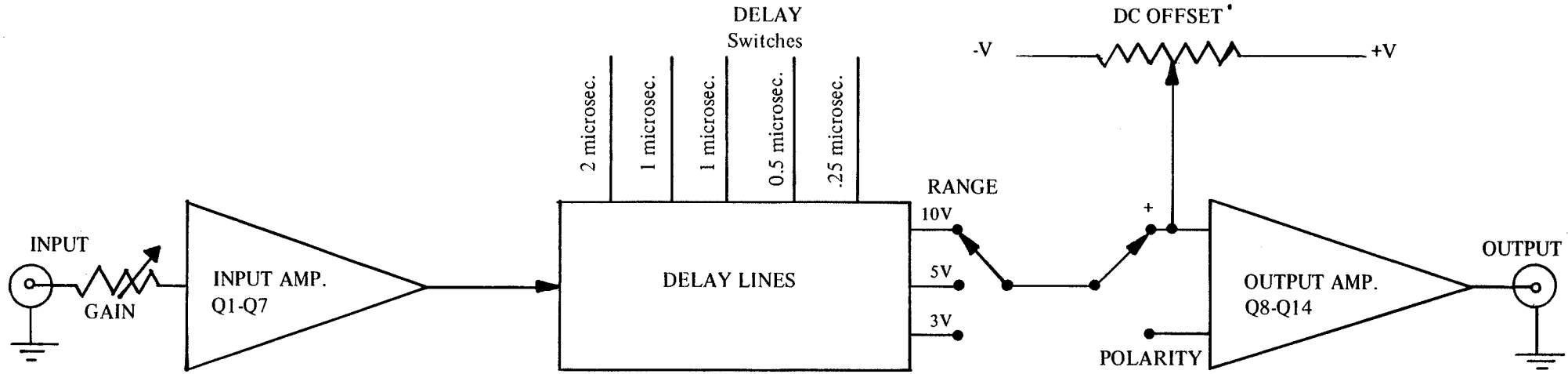

Figure 1. Block Diagram, Model 1457