CANBERRA

LOGIC SHAPER AND DELAY
Model 2055

Instruction Manual

Physics 191/297 laboratory

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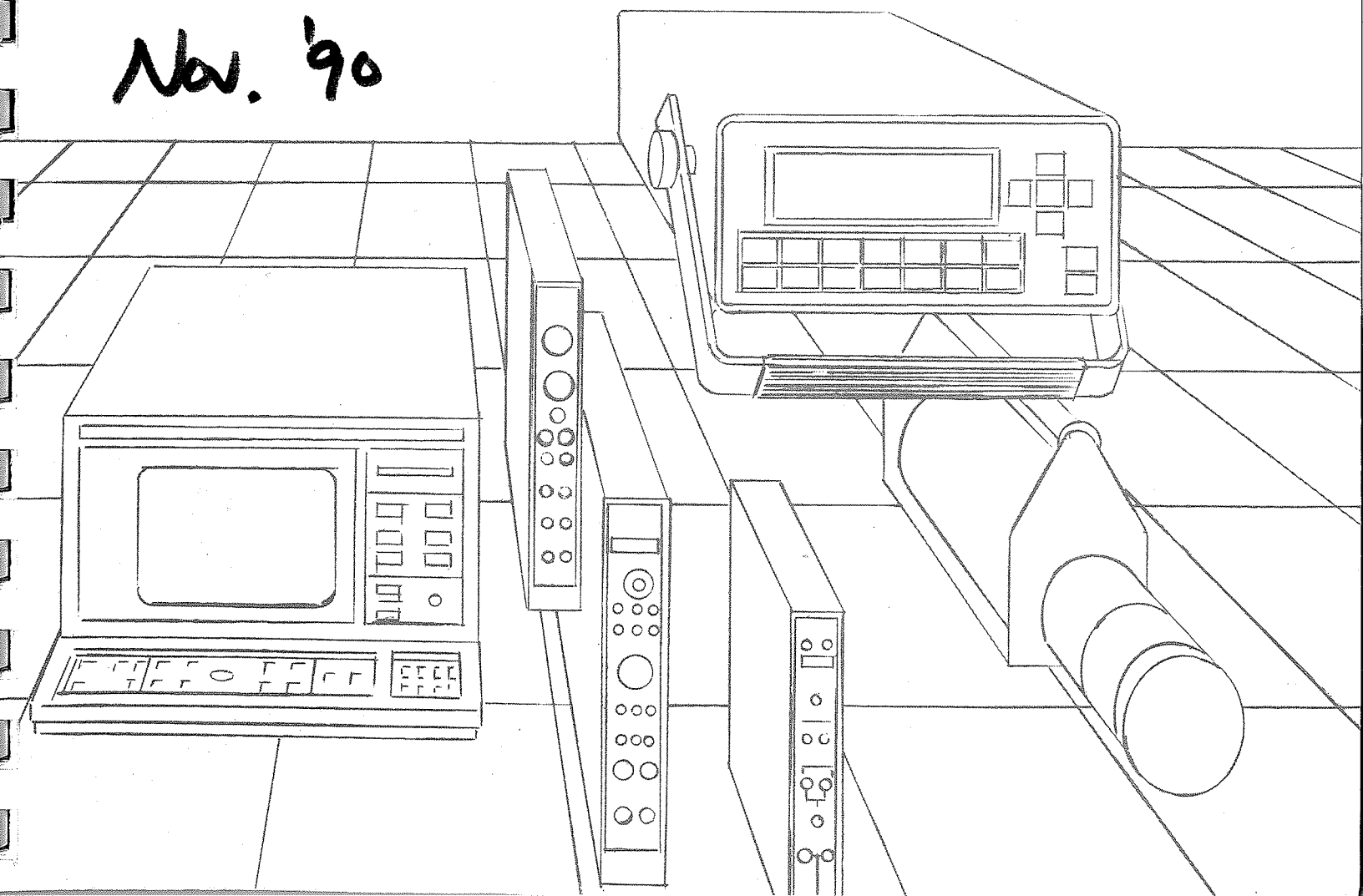

LOGIC SHAPER & DELAY
Model 2055

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LOGIC SHAPER & DELAY
MODEL 2055

Section 1
INTRODUCTION

The Model 2055 Logic Shaper and Delay offers versatility and performance. Its five simultaneous outputs offer solutions to many timing and logic interface problems. In addition input/output incompatability between instruments of different manufacture can be eliminated by the 2055.

Standard logic input pulses of either polarity generate the five simultaneous outputs for the experimenter's use. Separate positive and negative output logic signals are available with continuously adjustable delay, width and amplitude. Accompanying outputs include a Fast Negative NIM logic output following the selected delay time and a Period Output with its width equal to the delay time. Thus, logic signals meeting the input requirements of the Model 2055 may be reshaped and delayed up to 110 microseconds to provide maximum logic interface capability.

In timing applications, the multi-function 2055 compensates for inter-channel timing differences in fast/slow coincidence experiments. Since the PERIOD OUT is positive and negative, both coincidence and anticoincidence measurements can be performed.

The range of delay (0.1 to 110μs) allows the 2055 to be used in a wide variety of timing experiments from fast NIM logic applications to slow gas proportional detector anticoincidence measurements.

Typical interfacing applications are illustrated below:

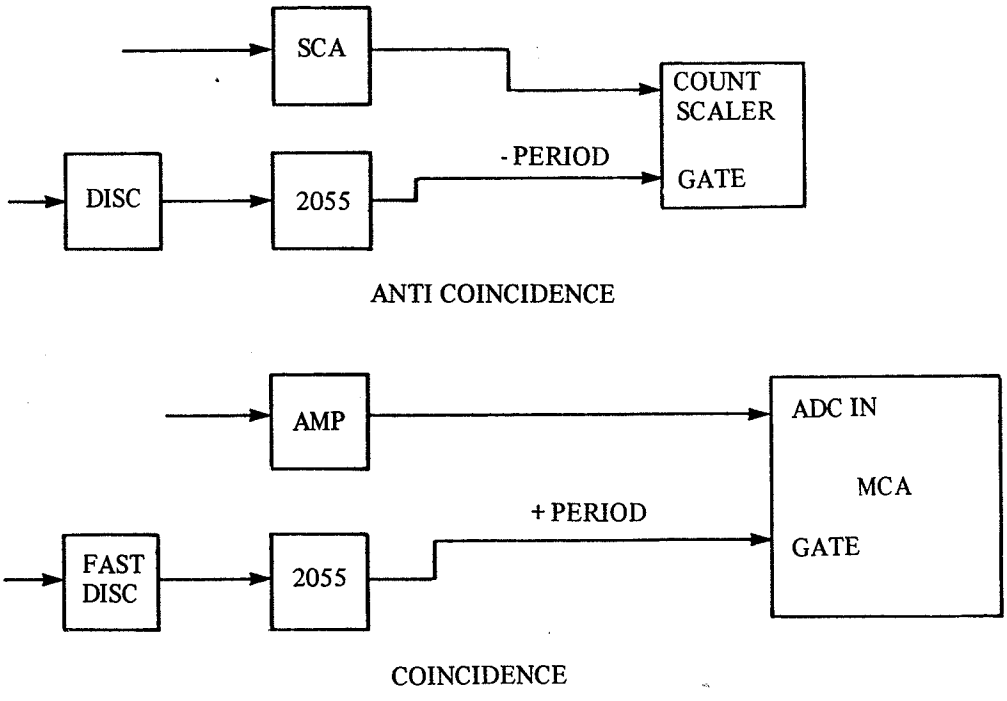


Figure 1-1. Typical Applications

Section 2
SPECIFICATIONS

2.1 INPUTS

INPUT

Accepts positive 0.7 to 12V or negative 0.4 to 12V NIM logic pulses
Rise time: any
Width: 20 nanoseconds minimum at +1V:
20 nanoseconds minimum at −1V
Z_{in}: ≈ 1K ohm, DC coupled, front/rear panel BNC connectors

2.2 OUTPUTS

POSITIVE

Logic pulse; variable amplitude range +2 to +10V
Width: Variable, 0.5 to 5μsec
Delay: Variable, 0.1 to 110μsec (plus propagation delay of approximately 75 nanoseconds)
Rise and fall time: ⩽ 25 nanoseconds
Z_{out}: ⩽ 25 ohms; short circuit protected, DC coupled, front panel BNC connector

NEGATIVE

Logic pulse characteristics identical to Positive output except for negative polarity

FAST

Standard fast negative NIM logic pulse: −800mV into 50 ohm load
Rise time: ⩽ 5 nanoseconds
Width: ≈ 20 nanoseconds
Z_{out}: 50 ohms; short circuit protected, DC coupled, front panel BNC connector

+ PERIOD

Logic pulse; amplitude ⩾ +4, ⩽ 5 Volts
Width: equal to selected Delay
Rise and fall time: ⩽ 25 nanoseconds
Z_{out}: ⩽ 25 ohms; short circuit protected, DC coupled, front panel BNC connector

− PERIOD

Logic pulse characteristics identical to + PERIOD output except inverted pulse excursion is to 0 to + 0.5 Volts from + 4 to 5 Volts.

Signal provided on front and rear panel BNC connectors.

2.3 CONTROLS

DELAY μsec

Front panel ten-turn precision locking potentiometer, continuously variable from 100 nanoseconds to 110μseconds (plus propagation delay ≈ 75 nanoseconds) in three overlapping ranges

MULTIPLIER	Front panel toggle switch to select DELAY potentiometer range of 0.1 to 1.1μsec, 1.0 to 11μsec, or 10 to 110μsec; X0.1, X1, and X10 positions
WIDTH	Front panel single-turn potentiometer to simultaneously adjust the Positive and Negative logic output widths; 0.5 to 5μsec range
AMPLITUDE	Front panel single-turn potentiometer to simultaneously adjust the Positive and Negative logic output amplitudes; 2 to 10V range
INPUT POS/NEG	Front panel toggle switch selects either Positive or Negative position to match logic input pulse polarity

2.4 PERFORMANCE

DELAY NONLINEARITY	Less than ± 0.5% of selected DELAY range
DELAY DRIFT	Less than ± 0.1%/°C of DELAY range selected
DELAY JITTER	Less than 0.02% of selected DELAY range
PULSE PAIR RESOLUTION	
DELAY MULTIPLIER X 10	DELAY Plus 10μs
DELAY MULTIPLIER X 1	DELAY Plus 1μs } When POS or NEG outputs used add WIDTH plus 1.5μs
DELAY MULTIPLIER X 0.1	DELAY Plus 0.5μs } When POS or NEG outputs used add WIDTH plus 1.5μs

2.5 CONNECTORS

INPUT, POS, NEG, FAST, +PERIOD, −PERIOD	Front panel, BNC, UG-1094/U
INPUT, NEG PERIOD	Rear panel, BNC, UG-1094/U

2.6 POWER

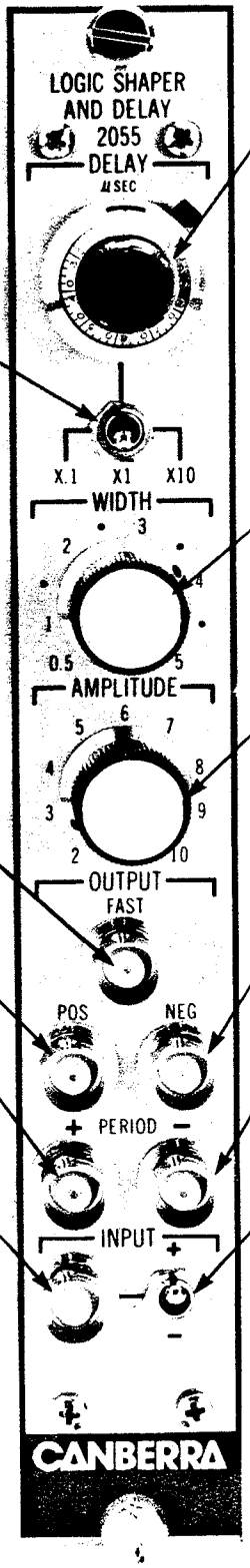
+24V	0mA
−24V	0mA
+12V	100mA
−12V	70mA

2.7 PHYSICAL

SIZE	Standard single-width NIM module (1.35 x 8.714 inches) per TID-20893 (Rev.)
WEIGHT	1.6 lbs. (0.7 kgs.)

Section 3
CONTROLS AND CONNECTORS

FRONT PANEL



R3
DELAY CONTROL
1.0 to 11μsec.

S1
DELAY MULTIPLIER
X0.1, X1, or X10 provides a total range of 0.1 to 110μsec

R4
OUTPUT PULSE WIDTH CONTROL
0.5 to 5μsec.

R5
OUTPUT PULSE AMPLITUDE
2 to 10 volts.

J1
FAST OUTPUT SIGNAL
−800mV into 50 ohms;
tr ≤5 nanosec;
tw ≈20 nanosec.

J2
NEGATIVE OUTPUT SIGNAL

J3
POSITIVE OUTPUT SIGNAL

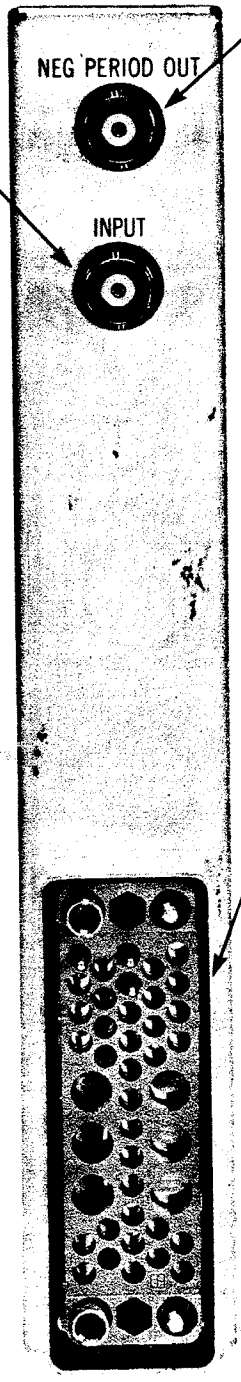
J4
−PERIOD
Logic Pulse - Zero: +4 to +5V.
One: 0 to +0.5V.
Width equal to delay

J5
+ PERIOD
Logic Pulse - Zero: 0 to +0.5V.
One: +4 to +5V
Width equal to delay.

S2
INPUT SIGNAL POLARITY SELECTOR

J6
INPUT SIGNAL
+0.7 to +12V, Width >20nsec
−0.4 to −12V, Width >20nsec
Z_{in} ≈1K ohms, DC coupled.

REAR PANEL



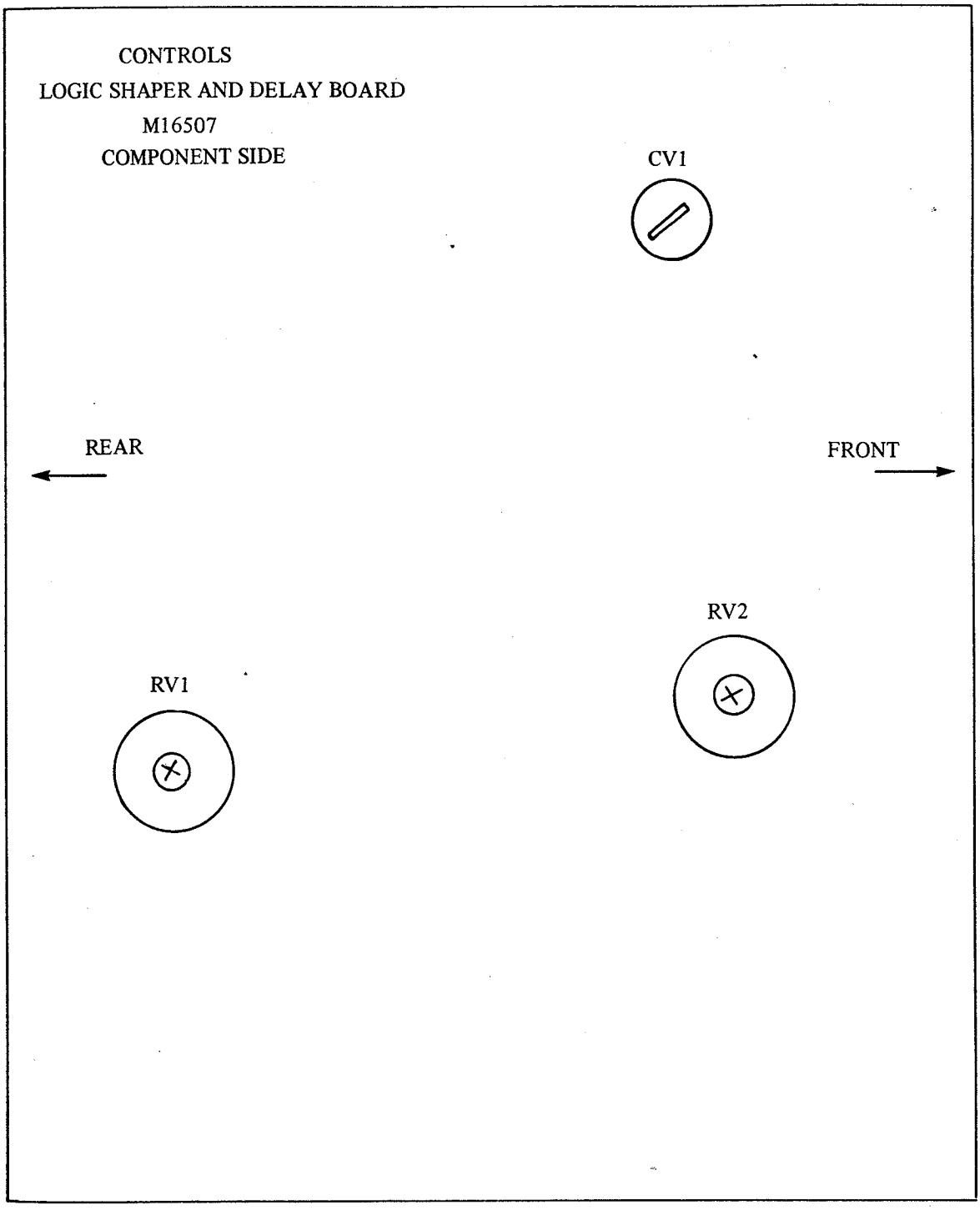
J101
NEG PERIOD OUT
Parallel Connection to J4, –Period.

J102
INPUT
Parallel Connection to J6, Input

J103
POWER
Connections used:

PIN	VOLTAGE
16	+12 Volts
17	–12 Volts
34	Ground

INTERNAL CALIBRATION CONTROLS



Section 4
OPERATING INSTRUCTIONS

4.1 GENERAL

1. The purpose of this section is to familiarize the user with the controls of the Model 2055 Logic Shaper and Delay and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

2. 50 ohm as well as 93 ohm coaxial cables and terminations may be utilized with the Model 2055.

4.2 INITIAL OPERATION

1. Insert the Model 2055 Delay Amplifier in on AEC compatible bin unit/power supply such as Canberra Model 2000. Set the Power switch to ON.

2. Set the 2055 Polarity Selector to Pos. Adjust a pulse generator for a +5.0 volt, 1 microsecond wide signal and connect it to the 2055 Input. Input rate to be < 5kHz.

3. Using an oscilloscope (use 93 ohm coax), monitor the Pos Output connector. Set the WIDTH control mid range and vary the AMPLITUDE control from CCW to CW and observe the pulse amplitude change from less than 2.0V to greater than 10.0V. The unterminated max. of 10.0V becomes 8.0V with 93 ohm termination and 7.5V at 50 ohm termination.

4. Set the AMPLITUDE control to mid scale and vary the WIDTH control. Terminate the cable in 93 ohms. When the WIDTH control is full CCW, the output pulse width should be less than 500 nanoseconds. Move WIDTH to full CW and observe the output signal width is 5 microseconds or greater.

5. Repeat Steps 3 and 4 observing the NEG Output signal.

6. Monitor the +PERIOD Output connector (terminate the cable with 93 ohms). Decrease the DELAY Control to full CCW. Set the Multiplier to X0.1. The output signal should be $\geqslant 4.0$ volts in amplitude and the width should be 100 nanoseconds. Turn DELAY to full CW and observe the output width should be 1.1 microseconds. Turn the DELAY control to 5.0 and observe the pulse width to be 0.5 microseconds. Switch the Multiplier to X1.0 and observe that the output width changes to 5.0 microseconds. Switch the Multiplier to X10 and observe that the output width changes to 50 microseconds.

7. Repeat Step 6 monitoring the - Period Output connector.

8. Monitor the Fast Output connector with the oscilloscope (terminate in 50 ohms). Trigger scope on the leading edge of +Period Output. Observe that Fast Output pulse occurs at end of Delay time setting. The pulse is approximately 20 nanoseconds wide and has a negative amplitude of 800mV.

4.3 INTERCONNECTIONS

Interconnecting between the various units in an experiment requires coaxial cables. These cables should be terminated resistively in their characteristic impedances. Failure to follow this requisite may result in ringing (several cycles of oscillation of varying amplitude at signal transition times) and/or spurious pulses appearing on the output. Both can initiate false triggering and subsequent erroneous experiment results.

INPUT and NEG PERIOD OUT on the rear panel are parallel connections to the front panel INPUT and –PERIOD output connectors, respectively. They are there to aid interconnecting to other units. Also, fewer cables to the front panel contributes to neatness of the installation.

5.6 FAST NEGATIVE CIRCUIT

This circuit provides a standard negative Fast NIM logic signal at the end of the delay period selected. The trailing edge of the delay monostable pulse is differentiated by CV1 (internal adjustment for setting the Fast negative output width) and R31. The negative portion of this pulse is fed to the drivers Q22 and Q23 and presented to the Fast Output BNC.

5.7 WIDTH MONOSTABLE

This monostable provides a means of adjusting the output width of the Positive and Negative Outputs. It consists of A2b, A2c, Q13, Q14 and is fired by the trailing edge of the delay monostable pulse. Q13, a current source, provides a constant current to the timing capacitor C9. By adjusting the Width control R4, the current to the timing capacitor is varied to change the time Q14 is ON and therefore the width of the monostable from 0.4 to 5 microseconds. RV2 is an internal adjustment to calibrate the Width control R4.

5.8 AMPLITUDE ADJUSTMENT CIRCUIT

This circuit controls the amplitude of the pulse, by a front panel Amplitude control, that is fed to the Negative and Positive Outputs. The output of the width monostable is fed through Q17. In the collector of Q17 is a voltage source Q18 which controls the amplitude of the pulse at the collector of Q17. This voltage is determined by R5, the Amplitude control. The pulse at the collector of Q17 is then fed to the Negative and Positive outputs through their buffers.

5.9 POSITIVE OUTPUT BUFFER

The Positive Output buffer provides a low impedance fast rise and fall time pulse with variable width and amplitude to the Positive Output BNC. This buffer is made up of a pair of complementary emitter followers Q15 and Q16.

5.10 NEGATIVE OUTPUT BUFFER

The Negative Output buffer provides a low impedance fast rise and fall time pulse with variable width and amplitude to the Negative Output BNC. This buffer is made up of an inverter Q19 and a pair of complementary emitter followers Q20 and Q21.

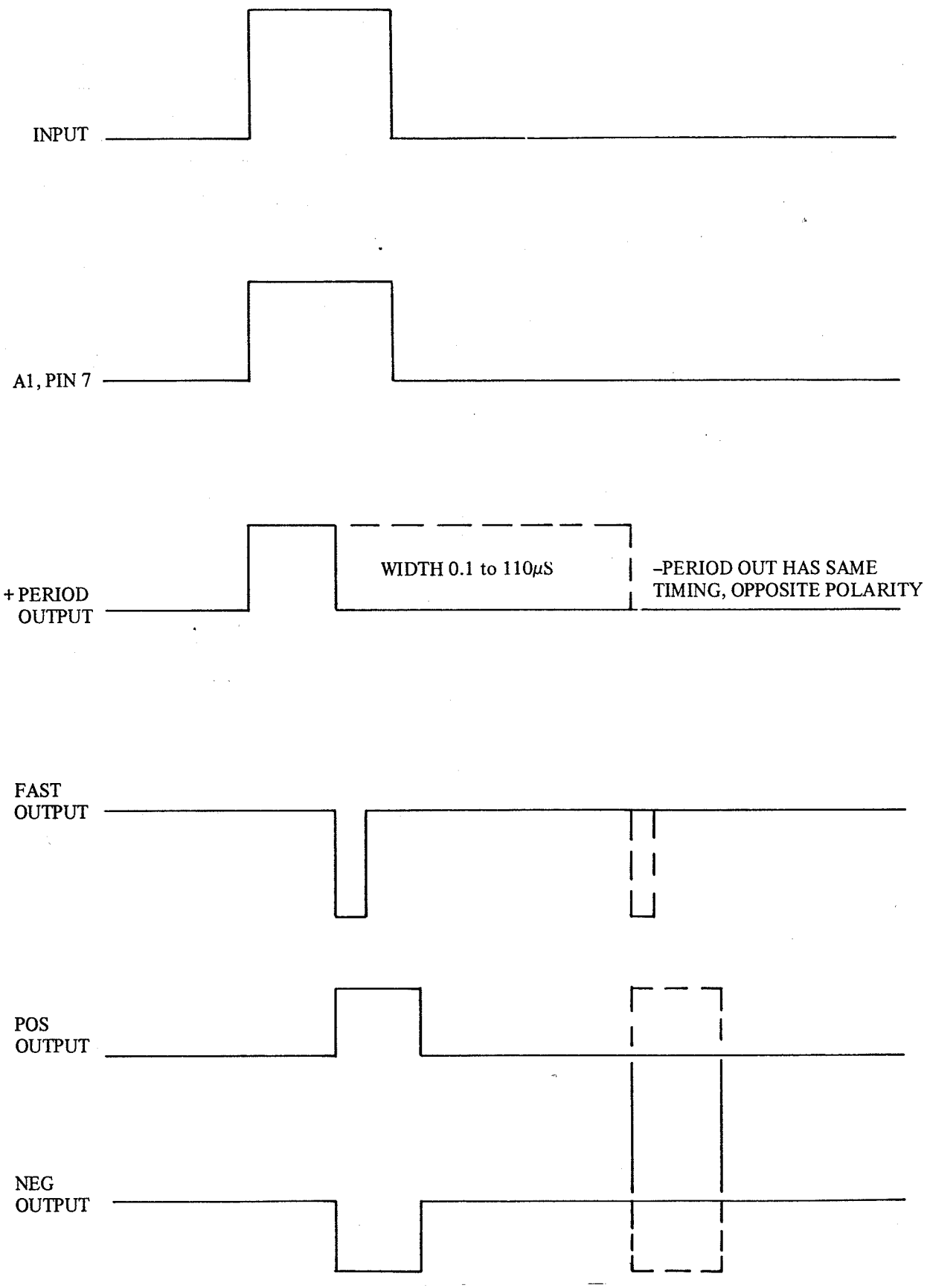


Figure 5-1. Model 2055 Timing Diagram

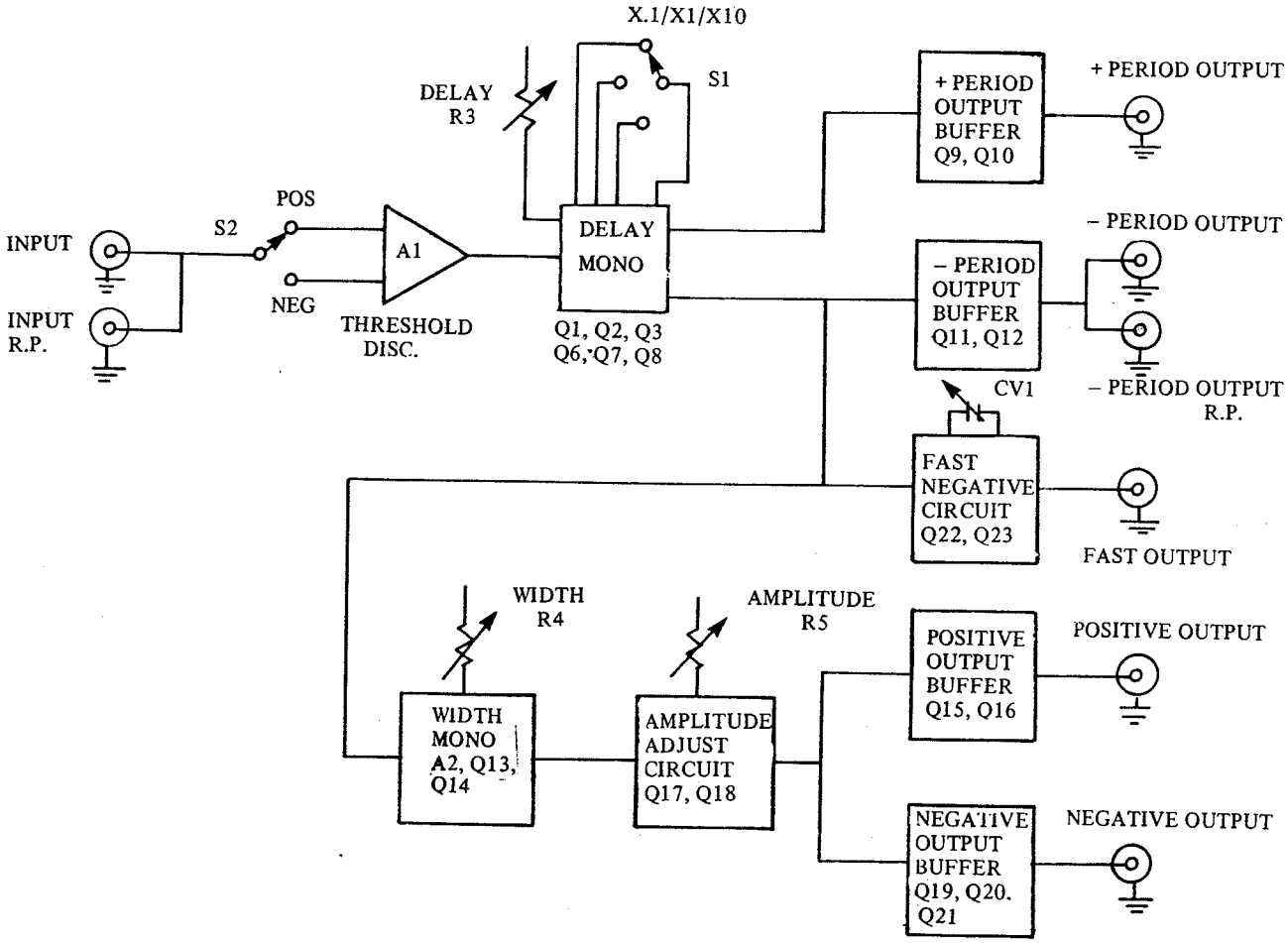


Figure 5-2. Model 2055 Block Diagram